Internal Memory Technology (Main Memory)

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References for This Lecture:

- William Stallings, Computer Organization and Architecture Designing For Performance, 9th Edition, Chapter 5 : *Internal Memory Technology*

Semiconductor Main Memory:

- The most common form of random-access storage for computer main memory, it volatile memory use semiconductor chips.

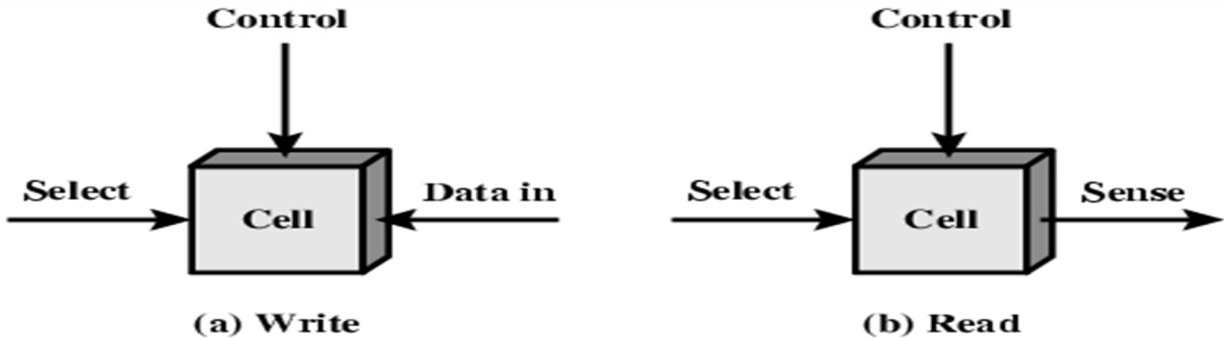
- The two basic forms of semiconductor random access memory are:
  - ✓ Dynamic RAM (DRAM); which used for main memory.
  - ✓ Static RAM (SRAM); which used for cache memory.
    - ❑ SRAM is faster, more expensive, and less dense than DRAM

Organization:

- The basic element of a semiconductor memory is the memory **cell**.
- Although a variety of electronic technologies are used ,all semiconductor memory cells share certain properties:
  - ✓ They exhibit **two stable states**, which can be used to represent binary 1 and 0.
  - ✓ They are capable of being **written** into (at least once), to set the state.
  - ✓ They are capable of being **read** to sense the state.

Memory Cell Operation

- The cell has three functional terminals capable of carrying an electrical signal:
  - ✓ The select terminal selects a memory cell for a read or writes operation.
  - ✓ The control terminal indicates read or write.
    - ❑ For writing, the other terminal provides an electrical signal that sets the state of the cell to 1 or 0.
    - ❑ For reading, that terminal is used for output of the cell's state.
- Figure below depicts the operation of a memory cell.



Random Access Memory (RAM):

- RAM is that; it is read data from the memory and to write new data into the memory easily and rapidly.
- RAM it is volatile.
- RAM must be provided with a constant power supply, if the power is interrupted, then the data are lost.
  - ✓ Thus, RAM can be used only as temporary storage.
- RAM technology is divided into two technologies:
  - ✓ Dynamic and static RAM.

DRAM and SRAM:

Dynamic RAM:

- A dynamic RAM (DRAM) is made with cells that store data as charge on capacitors.
- The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0. Because capacitors have a natural tendency to discharge, dynamic RAMs require periodic charge refreshing to maintain data storage.
- The term dynamic refers to this tendency of the stored charge to leak away, even with power continuously applied.

Static RAM:

- A static RAM (SRAM) is a digital device that uses the same logic elements used in the processor.
- In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations.
- A static RAM will hold its data as long as power is supplied to it.

SRAM vs DRAM

Dynamic RAM Properties	Static RAM Properties
Bits stored as charge in capacitors	Bits stored as on/off switches
Charges leak	No charges to leak
Need refreshing even when powered	No refreshing needed when powered
Simpler construction	More complex construction
Less expensive	More expensive
Need refresh circuits	Does not need refresh circuits
Slower	Faster
Used in Main memory	Used in Cache

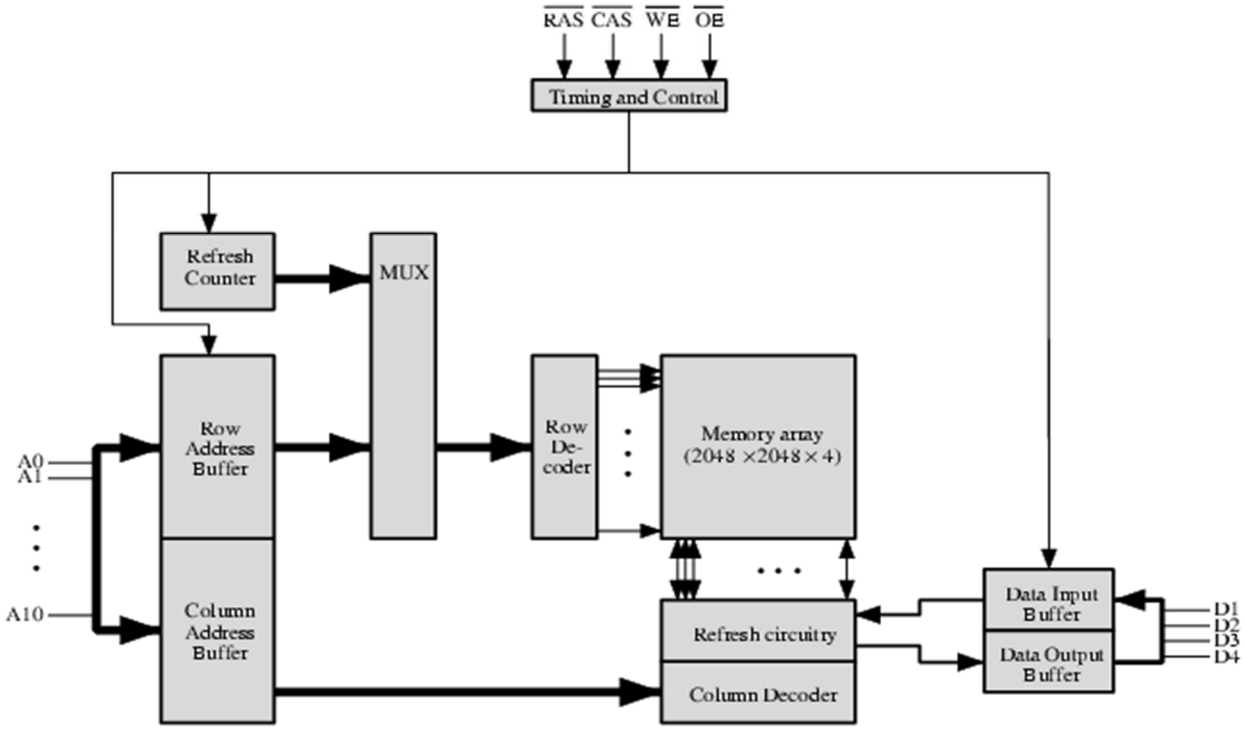
Chip Logic:

- As with other integrated circuit products, semiconductor memory comes in **packaged chips** .Each chip contains an array of memory cells.

- Speed, capacity, and cost these are effect on the organization of memory cells and functional logic on a chip.
- For semiconductor memories, one of the key design issues is the number of bits of data that may be read/write at a time.

- An organization in which the physical arrangement of cells in the array is the same as the logical arrangement of words in memory.
- The array is organized into W words of B bits each.
  - ✓ For example, a 16-Mbit chip could be organized as 1M 16-bit words.

- **Typical 16 Mb DRAM (4M x 4)**



- Above figure shows a typical organization of a 16-Mbit DRAM.
- In this case, 4 bits are read or written at a time.
- Logically, the memory array is organized as four square arrays of 2048 by 2048 elements. Various physical arrangements are possible.

- In any case, the elements of the array are connected by both horizontal (row) and vertical (column) **lines**.

- Each horizontal line connects to the Select terminal of each cell in its row; each vertical line connects to the Data-In/Sense terminal of each cell in its column.

- Address lines supply the address of the word to be selected.
  - A total of $\mathbf{\log_2 W}$ lines are needed.

- In our example, 11 address lines are needed to select one of 2048 rows.
  - These 11 lines are fed into a row decoder, which has 11 lines of input and 2048 lines for output.

- The logic of the decoder activates a single one of the 2048 outputs depending on the bit pattern on the 11 input lines (2^{11}= 2048).

- An additional 11 address lines select one of 2048 columns of 4 bits per column.

- Four data lines are used for the input and output of 4 bits to and from a data buffer.

- On input (write), the bit driver of each bit line is activated for a 1 or 0 according to the value of the corresponding data line.

- On output (read), the value of each bit line is passed through a sense amplifier and presented to the data lines.

- The row line selects which row of cells is used for reading or writing.

- Because only 4 bits are read/write to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

- There are only 11 address lines (A0–A10), half the number you would expect for a 2048* 2048 array. This is done to save on the number of pins. The 22 required address lines are passed through select logic external to the chip and multiplexed onto the 11 address lines.

- 11 address signals are passed to the chip to define the row address of the array, and then the other 11 address signals are presented for the column address. These signals are accompanied by row address select (RAS) and column address select (CAS) signals to provide timing to the chip.

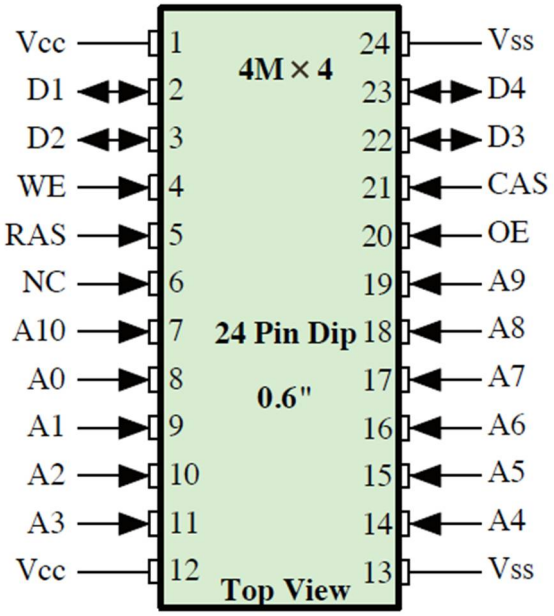
- The write enable (WE) and output enable (OE) pins determine whether a write or read operation is performed. Two other pins, not shown in Figure (2), are ground (Vss) and a voltage source (Vcc).

- All DRAMs require a refresh operation. A simple technique for refreshing is, in effect, to disable the DRAM chip while all data cells are refreshed.

Chip Packaging:

- An integrated circuit is mounted on a package that contains pins for connection to the outside world. A typical DRAM pin configuration is shown in Figure (3), for a 16-Mbit chip organized as 4M *4.

- Figure: Typical Memory Package Pins and Signals(**16-Mbit DRAM**)



- (A0–A10): The address of the word being accessed.
- (D1–D4): The data to be read out/write in.
- The write enable (WE) and output enable (OE) pins indicate whether this is a write or read operation. Because the DRAM is accessed by row and column, and the address is multiplexed, only 11 address pins are needed to specify the 4M row/column combinations ($2^{11} * 2^{11} = 2^{22}$ 4M).
- The functions of the row address select (RAS) and column address select (CAS) pins.
- The no connect (NC) pin is provided so that there is an even number of pins.
- The power supply to the chip (Vcc).
- A ground pin (Vss).